The Analysis of Dead Time on Switching Loss in High and Low Side MOSFETs of ZVS Synchronous Buck Converter

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***Abstract*—This work is about the analysis of dead time variation on switching losses in a Zero Voltage Switching (ZVS) synchronous buck converter (SBC) circuit. In high frequency converter circuits, switching losses are commonly linked with high and low side switches of SBC circuit. They are activated externally by the gate driver circuit. The duty ratio, dead time and resonant inductor are the parameters that affect the efficiency of the circuit. These variables can be adjusted for the optimization purposes. The study primarily focuses on varying the settings of input pulses of the MOSFETs in the resonant gate driver circuit which consequently affects the performance of the ZVS synchronous buck converter circuit. Using the predetermined inductor of 9 nH, the frequency is maintained at 1 MHz for each cycle transition. The switching loss graph is obtained and switching losses for both S_1 and S_2 are calculated and compared to the findings from previous work. It has shown a decrease in losses by 13.8 % in S_1. A dead time of 15 ns has been determined to be optimized value in the SBC design.**

***Keywords*— PSpice Simulation, Resonant Gate Driver, Synchronous Buck Converter, Switching Losses**

I. Introduction

In megahertz switching frequency, synchronous buck converter (SBC) circuit may contain losses which are normally caused by the high and low side switches. The resonant gate driver (RGD) circuit is applied due to its suitability in driving MOS-gated power switches in high frequency applications. High power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is used as a switch in this work of the proposed RGD circuit [1]. At present, there are various types of RGD circuits commercially available [2-4]. The resonant circuit transfers energy from the parasitic input capacitance of the power switching devices. This energy transfer prevents dissipation of the capacitive energy in the driver circuit which may otherwise destroy one or more components.

The resonant circuit includes an inductor in the driver circuit and one or more discrete capacitors are also included within the driver circuit to maintain resonance at a given frequency regardless of parasitic capacitance variation [5]. Although high frequency MOSFET is used, yet there are limitations in the design. When the frequency is increased, the gate driving losses will experience an increase in power dissipation. This in turn affects the performance of the converter. The duty ratio or pulse width, D, dead time, T_D, and the resonant inductor, L_r are the limiting parameters that influence the gate driver operation from conducting optimally. These parameters had been analyzed in [6] and the results show that the optimized values are found to be D = 20 %, T_D = 15 ns and L_r = 9 nH at 1 MHz switching frequency. However, the values of switching losses in the MOSFET are still very high. Therefore, the T_D parameter is adjusted to optimize switching losses. This is the primary objective in this work.

II. Proposed RGD-SBC Circuit

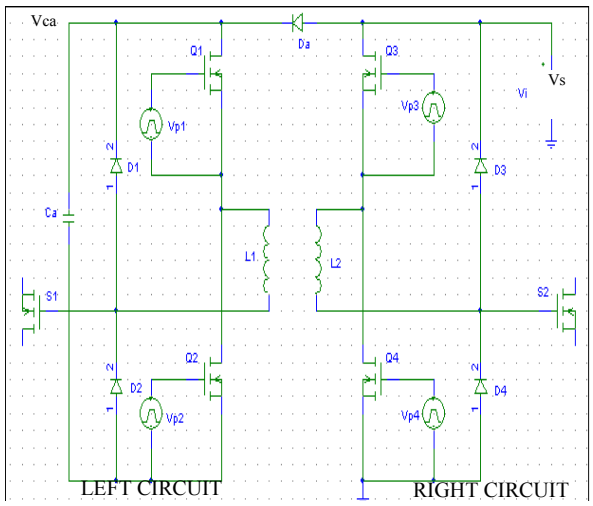


Figure 1. Proposed RGD Circuit

Fig. 1 shows the proposed RGD circuit which is used in this work. The circuit is suitable for SBC circuit because with a single input voltage, V_{in}, two output gate voltages will be generated complimentarily. Fig. 2 shows two output waveforms generated from an input voltage of the SBC circuit.

DOI: 01.ijcom.01.02.04

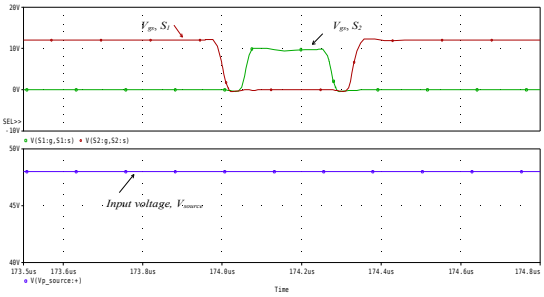
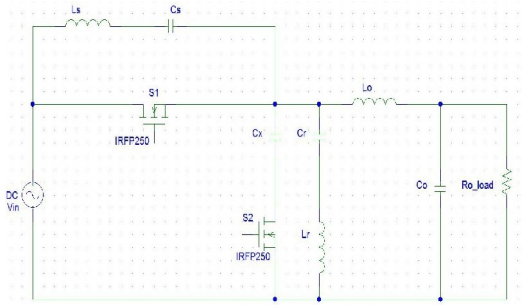


Figure 2. Gate Voltage of S_1 and S_2 & Input Voltage of SBC

As it can be seen, the left circuit of the proposed RGD circuit is the DC-RGD while the right circuit is just the symmetrical of the left circuit. The circuit has the advantages with simplicity having symmetrical pattern which gives better choice of component and parameter mo© 2010 ACEEEdification. In addition, a bootstrap circuit for high side driver [3] consisting of a diode, D_a and a capacitor, C_a are added into the circuit. The importance of bootstrap circuitry is that it aids in circuit simplification, symmetrical behavior and also minimizes switching loss. Besides that, it has less impact on the parasitic capacitance as well as better immunity in *dv/dt* turn-on. The proposed RGD circuit can conduct in two modes, complementary mode and symmetrical mode. In the complementary mode, it provides two drive signals with duty cycle *D* and *1-D*, respectively. This mode is suitable for driving two MOSFETs in a synchronous buck converter.

In the circuit, the four units of MOSFETs (Q_1, Q_2, Q_3, Q_4) settings will be reassigned carefully while other values which include oscillation frequency = 1 MHz, *D* = 20 % and L_r = 9 nH remain unchanged. Theoretically, when parameters of MOSFETS, Q_1 and Q_2 of the RGD circuit are changed, dead time of the left circuit, T_{D1} will vary. Similarly, when parameter values of Q_3 and Q_4 are changed, then dead time of the right circuit, T_{D2} will be also be modified. Consequently, the overall value of T_D in the proposed synchronous buck converter circuit as shown in Fig. 3 will also be modified. This gives result in new values of *D* and (*1-D*) in the synchronous buck circuit. S_1 is the high side switch while S_2 is the lower side switch and the switching losses of the circuit will be measured from these two switches. Overall, it is expected that the by varying the value of T_D, the performance of the SBC circuit will be affected, accordingly.



When the values of switching frequency equals to 1 MHz and L_r = 9 nH, together with the optimized value of T_D are unchanged, any changes in *D* will eventually result in different switching losses in the circuit.

III. Methodology

In this work, the proposed RGD-SBC circuit is simulated using PSpice software. The pulse settings of four MOSFETs in the proposed RGD circuit are modified carefully resulting in different values of T_D. The RGD circuit accordingly will affect the T_D of the synchronous buck converter circuit where the switching losses of the circuit are measured at the two MOSFET switches of S_1 and S_2. The results are then measured, compared and analyzed. The conclusion is then drawn.

IV. Results and Discussion

A. Proposed RGD Circuit

The dead time settings on each pulse generator in the proposed RGD circuit of Fig. 1 are shown in Table I while the pulse width settings are tabulated in Table II. Fig. 4 to Fig. 6 indicate the waveforms of dead time, delay time and pulse width.

TABLE I.
SETTINGS FOR DEAD TIME IN PROPOSED RGD CIRCUIT

Dead time		Initial delay time, $t_{d,initial}$ (ns)	Delay time for each voltage pulse			
T_D= T_{D1}= T_{D2} (ns)	T_{D3} (ns)		t_{d1} (ns)	t_{d2} (ns)	t_{d3} (ns)	t_{d4} (ns)
5	23	15	15	222	284	947
15	15	15	15	232	284	955
30	5	15	15	247	284	969

TABLE II
SETTINGS FOR PULSE WIDTH IN PROPOSED RGD CIRCUIT

Dead time	Pulse Width					
T_D= T_{D1}= T_{D2} (ns)	Vp_1 (ns)	Vp_2 (ns)	Vp_3 (ns)	Vp_4 (ns)	PW_{S1} (ns)	PW_{S2} (ns)
5	200	786	654	331	201	769
15	200	765	654	312	211	759
30	200	740	654	286	229	741

The dead times are varied in order to evaluate the performance of the circuit. For different dead times, the initial delay time, $t_{d,initial}$ is set to be constant at 15 ns. Therefore, the first delay time for voltage pulse one, t_{d1} is equal to $t_{d,initial}$. By taking T_D=15 ns as reference, it can be observed that only delay time for voltage pulse 1 and 3, t_{d1} and t_{d3} , and pulse width of voltage pulse of 1 and

DOI: 01.ijcom.01.02.04

3, PW_1 and PW_3, are changed in order to obtain the dead times of 5 ns and 30 ns. The table also shows that when T_{D1}=T_{D2} increases, T_{D3} decreases instead.

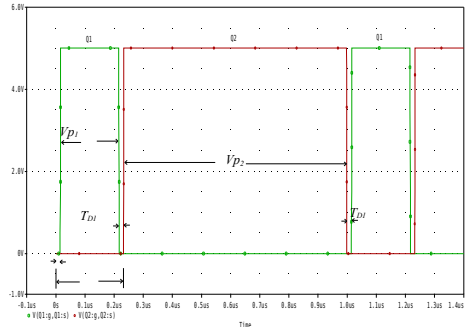


Figure 4. Indication of Pulse Width, Dead Time and Delay Time of Q_1 and Q_2 MOSFETs for T_D=15 ns

The graph of Fig. 4 is generated from the simulation of $V_{gs,Q1}$ and $V_{gs,Q2}$. Both Q_1 and Q_2 MOSFETs conduct complementarily to each other. The time when both MOSFETs are not conducting is known as the dead time, T_{D1}. Vp_1 is the pulse width of Q_1 and similarly to Vp_2, the pulse width of Q_2. $t_{d,\ initial}$ which is equal to t_{d1} is the initial delay time, set at a constant value of 15 ns. t_{d2} on the other hand is the delay time before Q_2 starts to conduct.

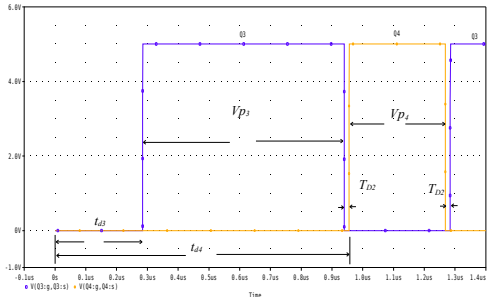


Figure 5. Indication of Pulse Width, Dead Time and Delay Time of Q_3 and Q_4 MOSFETs for T_D=15 ns

Fig. 5 shows the pulse width for Q_3, Vp_3 and Q_4, Vp_4. t_{d3} is the delay time before the MOSFET Q_3 starts to conduct. Similarly, t_{d4} is the delay time before Q_4 turns on. On the other hand, T_{D2} is the dead time when both MOSFETs, Q_3 and Q_4 are off.

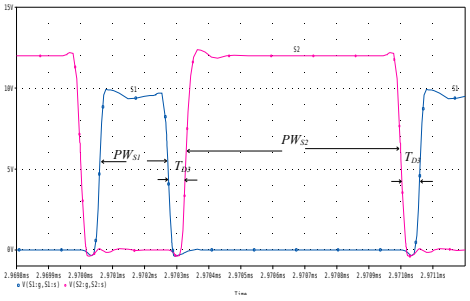


Figure 6. Indication of Pulse Width and Delay Time for S_1 and S_2 for T_D=15 ns

The gate source voltage of both switches, $V_{gs,S1}$ and $V_{gs,S2}$ is shown in Fig. 6. The maximum of $V_{gs,S1}$ is at 10 V and PW_{S1} is the pulse width of S_1. $V_{gs,S2}$ goes to a maximum value of 12 V with pulse width PW_{S2}. T_{D3} is the dead time when both switches are not conducting. Fig. 7 shows the operating waveforms generated from the left side of the proposed RGD circuit in Fig. 1.

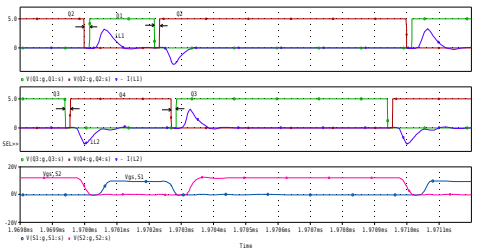


Figure 7. Operating Waveforms of Proposed RGD Circuit

Pulses from *Vp1* and *Vp2* are fed into the MOSFETS, Q_1 and Q_2 on the left side of RGD circuit. From the waveform, Q_1 and Q_2 are complementary driving pair inherited from the conventional driver. First, when Q_1 is switched on, the inductor current of the left circuit, i_{L1} starts to conduct and it is charged to maximum. The characteristic impedance of the resonant circuit can be represented by (1)

$$Z_o = \sqrt{\frac{L_R}{C_{in}}} \tag{1}$$

where L_R is the resonant inductor equivalent to 9 nH. The rise time t_r can be estimated by (2)

$$t_r = \frac{\pi}{2}\sqrt{L_R C_{in}} \tag{2}$$

The duration of this charging current depends on the value of L_R for being the time constant of the circuit. If the duration of the discharging current is not sufficient, it will cause current oscillation when Q_1 is turned off [1]. On the other hand, D_1 and D_2 are designed to clamp V_{gs} and to provide low impedance path for the inductor current and recover the driving energy which is represented by (3)

$$t_{rec} = \pi\sqrt{L_R C_{in}} \tag{3}$$

where C_{in} is the input gate capacitance of high side switch, S_1. On the other hand, the peak time is defined by (4)

$$t_{rec} = \frac{\tan^{-1}\left(\dfrac{2L_R \times \sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}}{R}\right)}{2\times\sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}} \tag{4}$$

After i_{L1} has been fully charged to peak current and at the same moment $V_{gs,S1}$ is clamped at V_{ca} by diode D_1, i_{L1} flows according to the path Q_1-L_1-$V_{gs,S1}$. The inductor current can be represented by equation (5).

$$i_{L1}(t_{peak}) = \frac{2V_{ca}}{\sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}} \cdot e^{-\frac{R_G}{2L_R}t} \cdot \sin\left(\frac{\sqrt{\dfrac{4L_R}{C_{in}} - {R_G}^2}}{2L_R} \cdot t\right) \tag{5}$$

DOI: 01.ijcom.01.02.04

i_{L1} then starts to discharge back to zero through $Q_{2,body\ diode}$-L_1-D_1 and back to V_{ca}, the direct voltage source at 12 V. After a predetermined T_D of either 5 ns, 10 ns or 15 ns, Q_2 will turn on instead. At this time Q_1 is turned off. Then i_{L1} starts to charge again but to a negative maximum value. This value will be a little lower compared to the positive value of i_{L1} because of leakage current. i_{L1} shows a symmetrical behavior compared to when Q_1 is conducting. When i_{L1} increases back to zero, it goes through D_2-L_1,-$Q_{1,body\ diode}$ and to V_{ca}. The symmetrical behavior in charging and discharging inductor current gives the total R_G power loss to be (6).

$$P_{loss\_R_G} = 2\times\int_{t_1}^{t_2}\left(i_{L1}{}^2 \bullet R_G\right)\bullet dt \approx \frac{R_G}{\left(R_G + Z_O\right)}\times Q_{DD}\times V_{ca}\times f_s \qquad (6)$$

The t_1 represents the rise time of the inductor current while t_2 is the recovery time of the inductor current. The same operation applies for the right hand side of the proposed RGD circuit in Fig. 1 with T_{D2} = 5 ns, 15 ns or 30 ns. The circuit can also be explained in terms of energy processing. When Q_1 is turned on, energy is transferred from the power source, V_{ca} to the resonant inductor and the gate capacitor. When V_{gs} of Q_1 reaches its peak, freewheeling of energy at inductor occurs. Then, the energy is returned to V_{ca}. Therefore, the proposed RGD demonstrates less power consumption compared to the conventional gate driver because of the energy recovery process.

The circuit also has the similar circuit operation for the discharging transition. When Q_2 is turned on, resonance takes place and the capacitive energy is transferred to the inductor. When i_{L1} starts to increase to the negative peak value, energy is merely freewheeling and finally, when the inductor current returns to zero, the inductor energy is also returned to the power source, V_{ca}. The right circuit operates in similar fashion to the left circuit but during different interval.

B. Proposed SBC Circuit

Referring to Fig. 3, S_1 is the high side switch and it has the primary function of a buck converter, used to convert high input voltage into low output voltage at the load. On the other hand, S_2 is the low side switch and it has a longer conduction time compared to S_1. The purpose is to lower the conduction loss in S_2. This can be verified by Table III.

TABLE III
SWITCHING LOSS FOR VARYING DUTY RATIO OF S2 AT T_D=15NS

Vgs, S_1 duty ratio , D	Vgs, S_2 duty ratio , D	S_1 Turn-off Peak (W)	S_2 Turn-on Peak (W)	S_1 Turn-off Switching Losses (W)	S_2 Turn-on Switching Losses (W)
20%	20%	91.617	109.726	1.603	2.195
20%	55%	87.060	98. 760	1.524	1.975
20%	70%	66.132	79.336	1.389	1.483
20%	75%	57.118	64.790	1.000	1.296

From the results, the duty ratio of S_2 at 75 % gives the lowest switching losses compared to other values. Therefore, it can be concluded that in order to reduce the conduction losses in the circuit, the conduction time of S_2 has to be optimized at 75 % for low switching loss.

These two switches conduct complementary to each other. Since both of them do not turn on at the same time, cross conduction will not occur. During T_D, when S_1 is turned off, the discharged inductor current at the load will flow into body diode S_2, which is also at its off condition. ZVS can be achieved if S_2 is completely turned off before S_1 is turned on. During the Discontinuous Current Mode (DCM) operation, the negative load inductor current can be applied where the body diode of S_1 is turned on first before the main body of the switch itself. Therefore, the switching losses at S_1 can be reduced since it has experienced ZVS. The operating waveforms of the proposed SBC circuit in simulation are shown in Fig. 8.

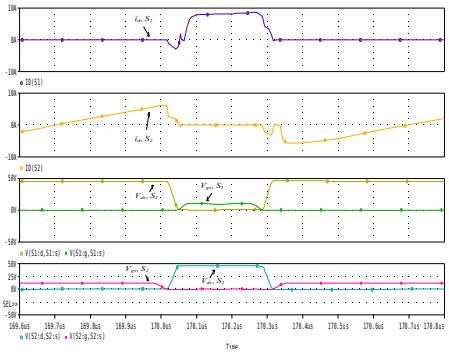


Figure 8. Operating Waveforms of SBC Circuit

From the waveforms, the operation of SBC circuit starts when S_1 starts to conduct while $i_{ds,S2}$ at its peak value starts to decrease to zero and turn off. At this time, it can be seen that $V_{ds,\ S2}$ starts to increase to its maximum value which is the V_{in} value of 48 V while $V_{ds,\ S1}$ works in complimentary pattern and reduces to zero. The scenario of $V_{ds,\ S2}$ going to its peak value while $V_{ds,\ S1}$ goes to zero should occur at the same time, in other words, there is no time interval. This is because of freewheeling phase of $i_{ds,\ S1}$. It causes $V_{gs,\ S1}$ to go to zero first before $V_{ds,\ S1}$ reaches its maximum value. For the drain current of S_1, it can be observed that $i_{ds,\ S1}$ starts to increase exponentially to its highest value. At this moment, the conduction of $i_{ds,\ S1}$ circulates through L_s and C_s in the SBC circuit.

S_1 stops conducting when it reaches its highest point. But at this moment, S_2 does not conduct yet. This indicates a dead time exists when there is a change in conduction of switches. At this time, $V_{ds,\ S1}$ starts to increase while $V_{ds,\ S2}$ starts to decrease. On the other hand, $i_{ds,\ S2}$ starts to decrease to its maximum negative value whereas $i_{ds,\ S1}$ is at zero. Following that, it can be seen from the figure $i_{ds,\ S2}$ starts to increase back to zero, which is like the previous state before it increases to its highest value while S_1 is off. At this moment, it can be observed that $i_{ds,\ S1}$ is at zero and $V_{ds,\ S1}$ is at its peak of the value V_{in}. This process repeats in the next subsequent cycles.

DOI: 01.ijcom.01.02.04

C. *Switching Losses of SBC at T_D = 15 ns*

The power losses of the circuit are interpreted by generating the turn-off switching loss waveform of S_1 and turn-on switching loss of S_2 as shown in Fig. 9.

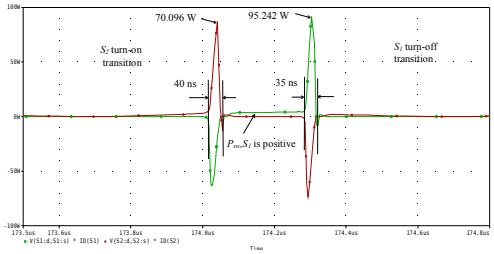


Figure 9. Turn-Off Switching Loss of S_1 and Turn-On Switching Loss of S_2

From the waveforms, the switching time for S_1 turn-off transition is 35 ns and for S_2, 40 ns. The calculation of switching losses is tabulated in Table IV and the evaluated results are compared with [1].

TABLE III
COMPARISON OF DATA [1] WITH THIS WORK AT T_D=15NS

	From [1]	From this work	% discrepancy
S_1 Turn-off Peak V_{ds} * I_{ds}	*65.000 W*	*57.118 W*	*- 13.80 %*
S_1 Turn-off Switching Losses	*1.138 W*	*1.000 W*	*- 13.80 %*
S_2 Turn-on Peak V_{ds} * I_{ds}	*95.000 W*	*64.790 W*	*- 46.63 %*
S_2 Turn-on Switching Losses	*1.100 W*	*1.296 W*	*+ 15.12 %*

From the results, it can be observed that the turn-off switching losses of S_1 have decreased. Otherwise, the problem of floating $V_{ds,S1}$ can cause the switching power loss to float as well. Conventionally, as most described in literature, the switching losses will be high and unfortunately they are ignored. The aim is to generate the drain voltage of less than 0.7 V during its turn-off or near to zero value during the entire turn-off transition time. Similarly to $V_{ds,S2}$, having a zero drain voltage can result in zero switching loss since their drain currents conduct at this time. This situation can be seen in the Fig. 10.

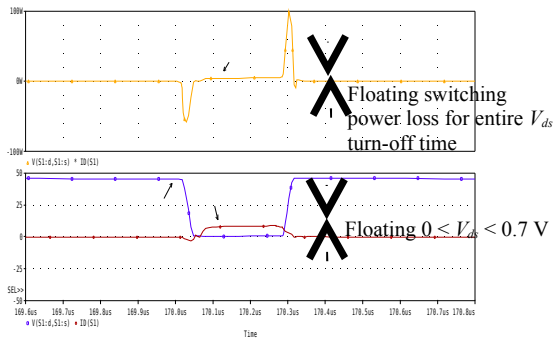


Figure 10. Floating Point of $V_{ds,S1}$

It can also be observed that the positive peak is higher than the negative. This shows that the power losses are not equally distributed in S_1. In the circuit, S_1 is dominant in generating the power loss of the SBC circuit. Thus, L_s and C_s has been added to the circuit in parallel with S_1 to solve this problem. Meanwhile, C_x has also been added in order to prevent the floating drain voltage of S_1. Hence, theoretically, L_s, C_s and C_x have to be varied to reduce the switching losses at S_1. However, S_2 turn-on switching losses have increased by 15.12 % compared to the study in [1]. Fig. 11 shows the operating waveforms for S_2.

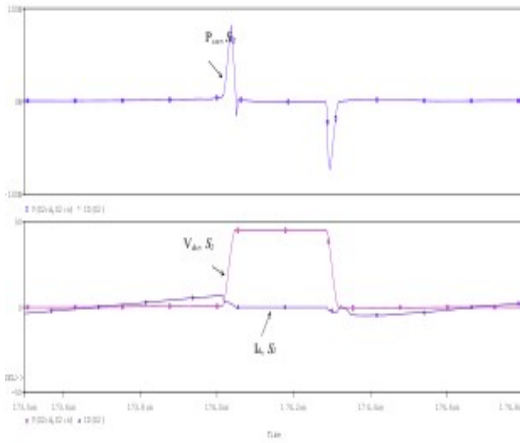


Figure 11. Operating Waveforms of S_2

Compared to S_1, there is no floating point at V_{ds}, S_2. As expected there is reduction in the turn-on switching losses and in return, the performance and reliability of the SBC circuit have improved.

D. *Comparison of Circuit Performance for Several T_{DS}*

With other parameter values remain unchanged except for T_D, the overall performance of the circuit is analyzed. The circuit performance at T_D =5 ns, 15 ns, and 30 ns is shown in Table V and Table VI.

TABLE I
PARAMETER EVALUATION FOR VARYING T_DS

T_D	V_{out} (V)	I_{out} (A)	t_{bd} (ns)	P_{COND} (W)	P_{BD} (W)
5ns	14.061	1.41	30	0.102	0.135
15ns	13.91	1.391	33	0.100	0.149
15 ns [1]	10.128	1.520	24	0.068	0.026
30ns	14.155	1.41	18	0.103	0.082

DOI: 01.ijcom.01.02.04

TABLE II
POWER LOSSES FOR VARYING T_DS

T_D	$P_{SW,S1}$ (W)	$P_{SW,S2}$ (W)	$P_{loss,total}$ (W)
5ns	1.538	1.145	2.920
15ns	1.000	1.296	2.296
15 ns [1]	1.138	1.100	2.238
30ns	1.707	1.823	3.7146

$P_{loss,total}$ is the total of all losses consisting conduction loss, P_{COND} , body diode loss, P_{BD} , and also switching losses, $P_{SW,S1}$ and $P_{SW,S2}$. From Table VII, it indicates that T_D at 15 ns gives the lowest total power loss, $P_{loss,total}$ of 2.296 W. Compared to T_D=5 ns and T_D=30 ns, T_D=15 ns is the most energy saving setting to be used. The switching losses, P_{SW} of the circuit are the major contributors of losses. P_{SW} comes from the two switches, S_1 and S_2, in the synchronous buck converter circuit. Theoretically, these losses can be reduced by reducing the switching time or peak power of both switches since P_{SW} =0.5*switching time*peak power*f_s. This means that the faster the MOSFETs can turn off, the more switching power can be reduced.

E. Results Verifications

Utilizing Mathcad, equations (2), (3) and (4) are used to obtain the theoretical values. The results are then compared with the values obtained using Pspice. All parameters are calculated and the comparison is shown in Table VII.

TABLE III
COMPARISON OF CALCULATION FROM MATHCAD & PSPICE AT T_D=15NS

Parameters	Method			% Δ
	Formula	PSpice	PSpice [1]	PSpice Calc.
Rise time, t_r (ns)	25.810	25.557	25.760	0.79
Recovery time, t_{rec} (ns)	51.620	58.041	56.645	2.46
Peak current, $i_{Lo}(t_{peak})$ (A)	3.572	3.367	3.970	15.19
Total switching loss, $P_{sw,total}$ (W)	2.296	2.820	2.240	25.89
Conduction loss, P_{COND} (W)	0.100	0.113	0.068	66.18
Body diode loss, P_{BD}(W)	0.149	0.134	0.025	436

The difference between the results obtained from PSpice done in this work and [1] show significant big margin. The work done in [1] shows lower P_{BD} since the proposed RGD design in Fig. 1 gives result in low body diode conduction time during T_D of 15 ns. This corresponds to the conduction loss of the switching MOSFETs as well. Other than these, the simulation results are acceptable. Nevertheless this work has successfully verified that 15 ns dead time is the best value to be used for the lowest switching loss in the converter.

V. CONCLUSION

In conclusion, switching losses in converter circuit are present due to high and low side switches operating in high frequency system. The gate driver circuit plays an important part in activating these switches. In order to reduce the losses, the dead time and duty ratio of the RGD circuit must be controlled. The PSpice software is used to implement this project. The switching losses for both S_1 and S_2 are calculated and compared to the findings from [1]. It has shown a decrease in losses by 13.8 % in S_1 but increase by 15.12 % in S_2, respectively. Moreover, further analyses and comparison of the circuit performance are also made and it can be concluded that T_D =15 ns is the best optimum value.

ACKNOWLEDGMENT

Authors would like to thank Universiti Teknologi PETRONAS, for providing financial support in presenting this work.

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DOI: 01.ijcom.01.02.04